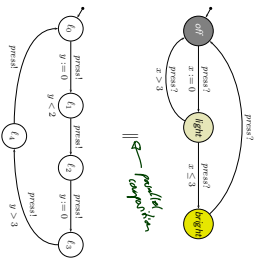


Example Cont'd



- Problems:**
- **Deadlock freedom** [Behrmann et al., 2004]
 - **Location Reachability** ("Is this user able to reach 'bright'?")
 - **Generative Reachability** ("Can this controller's clock go past 3?")

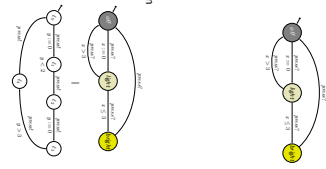
Channel Names and Actions

To define timed automata formally, we need the following sets of symbols:

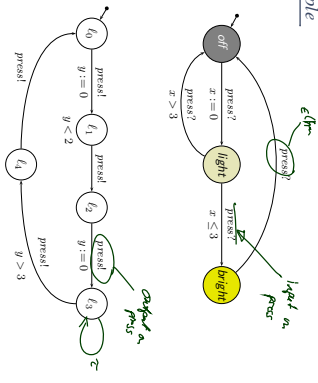
- A set $(a, b \in \Sigma)$ Chan of channel names or channels.
- For each channel $a \in \text{Chan}$, two visible actions: $a!$ and $a?$ denote input and output on the channel ($a! \notin \text{Chan}$).
- $\tau \notin \text{Chan}$ represents an internal action, not visible from outside.
- $(\alpha, \beta \in \Sigma) \text{ Act} := \{a! \mid a \in \text{Chan}\} \cup \{\tau\}$ is the set of actions.
- An alphabet B is a set of channels, i.e. $B \subseteq \text{Chan}$.
- For each alphabet B , we define the corresponding action set $B_{\text{TA}} := \{a! \mid a \in B\} \cup \{a? \mid a \in B\} \cup \{\tau\}$.
- Note: $\text{Chan}_{\text{TA}} = \text{Act}$.

Plan

- Pure TA syntax
- channel, actions
- (simple) clock constraints
- Def. TA
- Pure TA operational semantics
- clock valuation, time shift, modification
- operational semantics
- discussion
- Transition sequence, computation path, run
- Network of TA
- parallel composition (syntactical)
- restriction
- network of TA semantics
- Uppaal Demo
- Region abstraction, zones
- Extended TA; Logic of Uppaal



Example



Pure TA Syntax

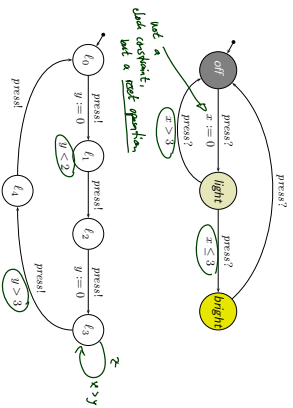
- Let $(x, y \in \Sigma) X$ be a set of clock variables (or clocks).
- The set $\varphi \in \Phi(X)$ of (simple) clock constraints (over X) is defined by the following grammar:

$$\varphi ::= x \sim c \mid x = y \sim c \mid \varphi_1 \wedge \varphi_2$$

where

 - $x, y \in X$,
 - $c \in \mathbb{Q}_+^+$, and
 - $\sim \in \{<, >, \leq, \geq\}$.

or can subtract
very difficult
if $X = \{x, y\}$, this can be done address for x30
- Clock constraints of the form $x - y \sim c$ are called difference constraints.



12.11

Timed Automaton

Definition 4.3. (Timed automaton)
 A (pure) **timed automaton** \mathcal{A} is a structure $\mathcal{A} = (L, B, X, I, E, f_{ini})$ where

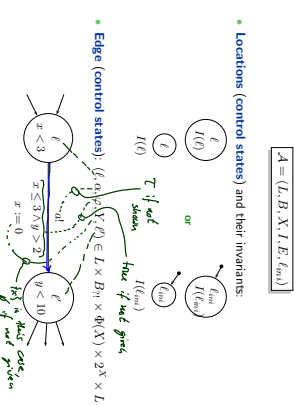
- $L \subseteq \Sigma$: L is a finite set of **locations** (or **control states**).
- $B \subseteq \text{Chan}$, **simple clock constraints** over X .
- X is a finite set of **clocks**.
- $I : L \rightarrow \Phi(X)$ assigns to each location a **clock constraint**, its **invariant**.
- $E \subseteq L \times B \times \Phi(X) \times 2^X \times L$: a finite set of **directed edges**.

Edges (l, g, X', l') from location l to l' are labelled with an **action** α , a **guard** g , and a set Y of clocks that will be **reset**.

f_{ini} is the **initial location**.

13.11

Graphical Representation of Timed Automata



14.11

Pure TA Operational Semantics

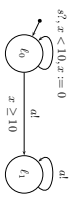
Clock Valuations

- Let X be a set of clocks. A **valuation** v of clocks in X is a mapping $v : X \rightarrow \text{Time}$ assigning each clock $x \in X$ the current time $v(x)$.
- Let φ be a clock constraint. The **satisfaction** relation between clock valuations v and clock constraints φ , denoted by $v \models \varphi$, is defined inductively:
 - $v \models x \sim c$ iff $v(x) \sim c$
 - $v \models x - y \sim c$ iff $v(x) - v(y) \sim c$
 - $v \models g_1 \wedge g_2$ iff $v \models g_1$ and $v \models g_2$

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 - $v \models g_1 \wedge g_2$ iff $v \models g_1$ and $v \models g_2$
- Two clock constraints φ_1 and φ_2 are called (**logically**) **equivalent** if and only if for all clock valuations v , we have $v \models \varphi_1$ if and only if $v \models \varphi_2$. In that case we write $\varphi_1 \iff \varphi_2$. (\models - \leftrightarrow - (φ_1, φ_2))

Example



References

References

[Behrmann et al., 2004] Behrmann, G., David, A., and Larsen, K. G. (2004). A tutorial on uppaal 2004-LTL. Technical report, Aalborg University, Denmark.
[Oderog and Dierks, 2008] Oderog, E.-R. and Dierks, H. (2008). Real-Time Systems - Formal Specification and Automatic Verification. Cambridge University Press.