### Real-Time Systems

# Lecture 9: DC Implementables II

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Gas Burner Controller: The Complete Specification C: { idle, people, "jourie, here. }

Gas Burner Controller: The Complete Specification

Gas Valve: (output)

Controller: (local)

 $\begin{array}{lll} \lceil \langle -G \rangle : \mathit{true} & (\mathsf{inht-4}) \\ \lceil G \wedge (\mathsf{dide} \vee \mathsf{purge}) \rceil & -f -G \rceil & (\mathsf{Syn-3}) \\ \lceil -G \wedge (\mathsf{ignite} \vee \mathsf{burn}) \rceil & -f \mid G \rceil & (\mathsf{Syn-4}) \\ \lceil G \rceil : \lceil -G \wedge (\mathsf{idle} \vee \mathsf{purge}) \rceil & -f \mid G \rceil & (\mathsf{Stab-6}) \end{array}$ 

CORREST, CO Controller: (local) 3.507 3.607 3.607 3.607 4.607

 $\lceil \neg G \rceil : \lceil G \wedge (\mathsf{ignite} \vee \mathsf{bum}) \rceil \longrightarrow \lceil G \rceil$  (Stab-7)  $\lceil \neg G \wedge (\mathsf{idle} \vee \mathsf{purge}) \rceil \longrightarrow_0 \lceil \neg G \rceil \\ (\mathsf{Stab-6-init})$ 

Flame: (input) Heating Request: (input)

 $| | \lor [\neg H] ; true,$  (Init-2)

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### Content

- Correctness Proof for the Gas Burner Implementables
- Now where's the implementation?
- Programmable Logic Controllers (PLC)
  He How do they look like?
  What's special about them?
  The read/compute/write cycle of PLC
- (\* Structured Text example (\* Other IEC 61131-3 programming languages Example: Stutter Filter
- -(\* Example: Stutter Filter
  -(\* PLCA Semantics by example
  -(\* Cycle time PLC Automata

Recall: Specification of a Gas Burner Controller

Implementable Gas Burner Controller:
Correctness Proof

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where A(c) constrains the reaction time of computers executing the control program. Reach it a program behaving like (GS-Ctrl is executed on a computer with reaction time z such that A(c) holds, then Req is \underbrace{subtiged}_{z} in the system. Recall:

Req : \Longleftrightarrow \Box(\ell \geq 00 \implies 20 \cdot f L \leq \ell)
and (cf. Olderog and Dierks (2008))
\underbrace{Req.1 \implies Req}_{z}
for the simplified requirement
Req.1 := \Box(\ell \leq 30 \implies f L \leq 1).
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Lemma \begin{tabular}{ll} Lemma \begin{tabular}{ll} Lemma \begin{tabular}{ll} $J(G) = 0 \\ $| G(G) = 0 \\ $| C(G) = 0 \\ $| C(G)
```

we can directly conclude  $\mathcal{I}, \mathcal{V}, [b,e] \models \ell \leq 0.5 + \varepsilon.$ 

 $\lceil \mathsf{ignite} \rceil \stackrel{0.5+\varepsilon}{\longrightarrow} \lceil \neg \mathsf{ignite} \rceil$ 

(Prog-2)

Thus  $\mathcal{I}, \mathcal{V}, [b,e] \models f \neg F \leq 2\varepsilon$ .

 $\mathcal{I}, \mathcal{V}, [b, e] \models \overline{\square \Big( [-F] \implies \ell \leq \varepsilon \Big)} \wedge \overline{-\Diamond ([F] : [-F] : [F])} \\ \xrightarrow{\text{by (Sym-2)}}$ 

Lemma 3.15 Cont'd

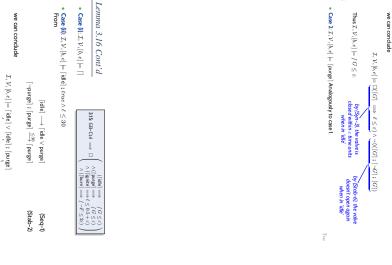
 $\begin{array}{c} \mathsf{GB\text{-}Ctrl} \implies \Box & (\lceil \mathsf{Ide} \rceil \implies f G \leq \varepsilon) \\ \land (\lceil \mathsf{purge} \rceil \implies f G \leq \varepsilon) \\ \land (\lceil \mathsf{gante} \rceil \implies \ell \leq 0.5 + \varepsilon) \\ \land (\lceil \mathsf{bunn} \rceil \implies f \neg F \leq 2\varepsilon) \end{array}$ 

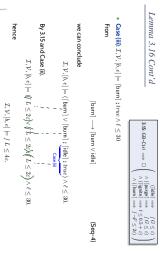
Gas Burner Controller Correctness Proof

 $\mathbf{Set}\,\mathsf{GB-Ctrl}:=\mathsf{Init-1}\wedge\cdots\wedge\mathsf{Stab-7}\wedge\varepsilon>0.$ 

In the following, we show

 $\models \mathsf{GB\text{-}Ctrl} \land A(\varepsilon) \implies \mathsf{Req\text{-}1}.$ 





Thus  $\varepsilon \leq 0.5$  is sufficient for Req-1 (  $fL \leq 1$  ) in this case.

Thus  $\boxed{\varepsilon \leq 0.25}$  is sufficient for Req-1 ( $f L \leq 1$ ) in this case.

 $\mathcal{I}, \mathcal{V}, [b, e] \models (\mathcal{I} L \leq \varepsilon) \vee (\mathcal{I} L \leq \varepsilon : \mathcal{I} L \leq \varepsilon)$ 

 $\mathcal{I}, \mathcal{V}, [b,e] \models \mathit{f} L \leq 2\varepsilon$ 

### Lemma 3.16 Cont'd

 $\mathbf{315.\,GB\text{-}Ctrl} \implies \Box \begin{pmatrix} \land (\lceil \mathsf{ide} \rceil \implies fG \leq \varepsilon) \\ \land (\lceil \mathsf{purge} \rceil \implies fG \leq \varepsilon) \\ \land (\lceil \mathsf{gurite} \rceil \implies \ell \leq 0.5 + \varepsilon) \\ \land (\lceil \mathsf{burn} \rceil \implies f \neg F \leq 2\varepsilon) \end{pmatrix}$ 

Case (iv):  $\mathcal{I}, \mathcal{V}, [b,e] \models [\text{ignite}] : true \land \ell \leq 30$  From

 $\lceil \mathsf{ignite} \rceil \longrightarrow \lceil \mathsf{ignite} \vee \mathsf{burn} \rceil$ 

(Seq-3)

By 3.15 and Case (iii).  $\mathcal{I}, \mathcal{V}, [b,e] \models (\lceil \mathsf{ignite} \rceil \lor \lceil \mathsf{ignite} \rceil : \underbrace{\lceil \mathsf{burn} \rceil : \mathit{true}}_{l}) \land \ell \leq 30.$ 

 $\mathcal{I}, \mathcal{V}, [b,e] \models (\not [L \le 0.5 + \varepsilon) \lor \not [L \le 0.5 + \varepsilon); \not [L \le 4\varepsilon) \land \ell \le 30$  $\mathcal{I}, \mathcal{V}, [b, e] \models \int L \leq 0.5 + 5\varepsilon$ .

Thus  $\varepsilon \leq 0.1$  is sufficient for Req-1 ( $\int L \leq 1$ ) in this case.

Lemma 3.16 Cont'd

315: GB-Ctrl ⇒ □  $\square \left( \begin{array}{c} (\lceil \operatorname{idle} \rceil \Longrightarrow f \, G \leq \varepsilon) \\ \wedge (\lceil \operatorname{purge} \rceil \Longrightarrow f \, G \leq \varepsilon) \\ \wedge (\lceil \operatorname{lignite} \rceil \Longrightarrow \ell \leq 0.5 + \varepsilon) \\ \wedge (\lceil \operatorname{burm} \rceil \Longrightarrow f \neg F \leq 2\varepsilon) \end{array} \right)$ 

 $\bullet \ \ \mathbf{Case} \ \ (\mathbf{V}) \colon \mathcal{I}, \, \mathcal{V}, \, [b,e] \mid = \lceil \mathsf{purge} \rceil \ ; \, true \land \ell \leq 30 \\ \mathsf{From} \ \ \,$ 

 $\lceil \mathsf{purge} \rceil \longrightarrow \lceil \mathsf{purge} \vee \mathsf{ignite} \rceil$ 

(Seq-2)

 $\mathcal{I}, \mathcal{V}, [b, e] \models \int L \leq 0.5 + 6\varepsilon.$ 

and 3.15 and Case (iv) we can conclude

Thus  $\varepsilon \leq \frac{1}{12}$  is sufficient for Req-1 ( $\int L \leq 1$ ) in this case.

 $\models \exists \varepsilon \bullet \mathsf{GB-Ctrl} \implies \underline{\Box(\ell \leq 30 \implies fL \leq 1)}_{\mathsf{Reg-1}}$ 

Discussion

Discussion

We used only

for instance? What about

 $\mathsf{Prog-1} = \lceil \mathsf{purge} \rceil \xrightarrow{30+\varepsilon} \lceil \neg \mathsf{purge} \rceil$ 

'Seq-1.' Seq-2.' Seq-3.' Seq-4.'
'Prog-2.' 'Syn-2.' 'Syn-3.'
'Stab-2.' 'Stab-5.' 'Stab-6.'

We used only

'Seq-1', 'Seq-2', 'Seq-3', 'Seq-4', 'Prog-2', 'Syn-2', 'Syn-3', 'Stab-2', 'Stab-5', 'Stab-6',

What about

for instance?

 $\mathsf{Prog-1} = \lceil \mathsf{purge} \rceil \xrightarrow{30+\varepsilon} \lceil \neg \mathsf{purge} \rceil$ 

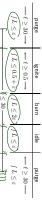
We only proved the safety property on testage. we did not consider the (not formalised) liveness requirement: the controller should do something finally, e.g. heating requests should be served finally by trying an ignition.

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### Correctness Result

Theorem 3.17.  $\models \left(\mathsf{GB\text{-}Ctrl} \land \varepsilon \leq \frac{1}{12}\right) \implies \mathsf{Req}$ 

- $\bullet \ \ \mathsf{Req-1} = \Box(\ell \leq 30 \implies \int L \leq 1) \ \mathsf{implies} \ \mathsf{Req}.$   $\bullet \ \ \mathsf{315} \ [\mathsf{purge}] \implies \int L \leq \varepsilon. \ [\mathsf{sgnite}] \implies \int L \leq 0.5 + \varepsilon. \ [\mathsf{burn}] \implies \int L \leq 2\varepsilon. \ [\mathsf{idle}] \implies \int L \leq \varepsilon.$



• Thus  $\int L \leq 0.5 + 6\varepsilon$ , so a sufficient reaction time constraint is  $A(\varepsilon) := \varepsilon \leq \frac{1}{12}$ .

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- Example Stutter Filter
   Structured Text example
   Other IEC 61131-3 programming languages
- PLC Automata
- → e Example: Stutter Filter
  → PLCA Semantics by example
  → Cycle time

Content

Example: Stutter Filter
 Structured Text example
 Other IEC 61131-3 programming languages

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 PLCA Semantics by example
 Cycle time

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What is a PLC?

Correctness Proof for the Gas Burner Implementables

Now where's the implementation?
Programmable Logic Controllers (PLC)
Programmable Logic Controllers (PLC)
Programmable Logic Controllers (PLC)
Programmable Logic Controllers (PLC)
Programmable Logic Computer write cycle of PLC
Programmable Logic Controllers (PLC)
Pr

Now Where's the Implementation?

Full DC DC Implementables | Reg | Prove | Disk

PLC-Automata IEC 61131-3 Binary

The Plan

The Plan

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How do PLC look like?

What's special about PLC?

- n microprograssor.
  memory times

   digital for analog I/O ports

   possibly RS 232.
  fieldbuses, networking

   robust hardware

   reprogrammable

   standardised pto orgamming
  model (IEC 61131-3)

## Where are PLC employed?



- mostly process
   automatisation
   production lines
   padaging lines
   derintal plants
   power plants
   power plants
   electric motors,
   pneumatic or hydraulic
   cylinders

  ...
- not so much: product automatisation, there
- tailored or OTS controller boards
   embedded controllers

Example: Stutter Filter

How are PLC programmed, practically?

Example: reliable, stutter-free train sensor.

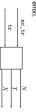
 Assume a track-side sensor which outputs: no\_tr - iff "no passing train"
tr - iff "a train is passing"

Problem: the sensor may stutter,
 i.e. oscillate between "no\_tr" and "tr" multiple times.

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Assume that a change from "no\_tr" to "tr" signals arrival of a train. (No spurious sensor values.)

 $\bullet$  Idea: a stutter filter with outputs N and  $T_\circ$  for "no train" and "train passing" (and possibly  $X_\circ$  for error).

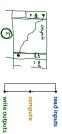


After arrival of a train, it should ignore " $no_tx$ " for 5 seconds.



## How are PLC programmed?

PLC have in common that they operate in a cyclic manner.



- Cyclic operation is repeated until external interruption (such as shutdown or reset).
   Cycle time: typically a few milliseconds (Lukoschus, 2004).
- Programming for PLC means providing the "compute" part. Input/output values are available via designated local variables

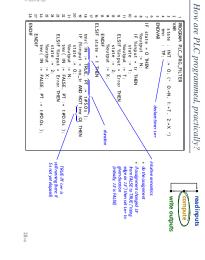
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How are PLC programmed, practically? WY WE : NT := 0, (\* 0 = N, 1:=T, 2 = X\*)

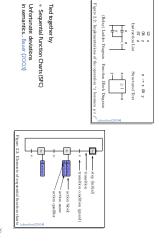
BOOMS | TP.

BO PROGRAM PLC\_PRG\_FILTER
VAR compute write outputs

28/-0



# Alternative Programming Languages by IEC 61131-3



Tell Them What You've Told Them...

We can prove the Gas Burner jriplementables correct by carefully considering its phases.
A crucial aspect is reaction time:

References

have a real-time dock device.
 can read inputs and write outputs.
 can manage local state.

Programmable Logic Controllers (PLC)
 are epitomic for real-time controller platforms:

some platforms may be too slow to satisfy requirements.

Controller programs executed on some hardware platform do not react in 0-time,

PLC programs

are executed in read/compute/write cycles,
 have a cycle-time (possibly a watchdog).

PLC Automata are a more abstract (than IEC 61131-3) way of describing and studying PLC programs.

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PLC Automata

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 Cycle time

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Lukoschus, B. (2004). Compositional Verification of Industrial Control Systems. PhD thesis, Christian-Albrechts-Universität zu Kiel.

Bauer, N. (2003). Formale Analyse von Sequential Function Charts. PhD thesis, Universität Dortmund.

References

Olderog, E.-R. and Dierks, H. (2008). Real-Time Systems - Formal Specification and Automatic Verification Cambridge University Press.

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