## **Real-Time Systems**

http://swt.informatik.uni-freiburg.de/teaching/SS2014/rtsys

## Exercise Sheet 5

Early submission: Tuesday, 2013-07-21, 10:00 Regular submission: Wednesday, 2013-07-22, 10:00

Exercise 1: Region Construction [2]

(10/20 Points)



Figure 1: Timed Automaton for Exercise 1.

Consider the timed automaton  $\mathcal{A}$  in Figure 1. In the tutorial, we had the impression that locations  $\ell_2$  and  $\ell_3$  are not reachable.

Prove this statement by constructing the region automaton.

*Hint:* you need not present all configurations of  $\mathcal{R}(\mathcal{A})$  if you explain appropriately why those, which you do present, are sufficient.

## Exercise 2: Zone Construction [2]

(5/20 Points)



Figure 2: Zone  $\varphi_0$  for Exercise 3.

Compute

 $\operatorname{Post}_{e}(\ell_{0}, z)$ 

for the zone  $\varphi_0$  given by Figure 2 and for both edges originating at  $\ell_0$ ; give the intermediate steps up to  $\varphi_5$ .

What can you conclude about the reachability of  $\ell_1$  and  $\ell_2$ ? You may represent zones graphically or symbolically.

## Exercise 4: Deadlock

 (i) Please give (possibly from (correctly cited) literature) an exact formal definition of deadlock in Uppaal [1], i.e. please explain (formally) using the notions and definitions from the lecture when exactly a network of timed automata satisfies

## ${\tt E} <> {\tt deadlock}.$

Consider the following examples:



## (5/20 Points)



- (ii) How does deadlock relate to timelock? (1/5)
- (iii) What is checking for deadlocks good for? (1/5)

# References

- [1] Gerd Behrmann, Alexandre David, and Kim G. Larsen. A tutorial on uppaal 2004-11-17. Technical report, Aalborg University, Denmark, November 2004.
- [2] Ernst-Rüdiger Olderog and Henning Dierks. *Real-Time Systems Formal Specification and Automatic Verification*. Cambridge University Press, 2008.