

Real-Time Systems

Lecture 8: DC Properties II

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Contents & Goals

Last Lecture:

- DC Implementables

This Lecture:

- **Educational Objectives:** Capabilities for following tasks/questions.

- Facts: (un)decidability properties of DC in discrete/continuous time.
- What's the idea of the considered (un)decidability proofs?

Content:

- DC Implementables Cont'd
- RDC in discrete time
- Satisfiability and realisability from 0 is decidable for RDC in discrete time
- Undecidable problems of DC in continuous time

DC Implementables Cont'd

Recall: DC Implementables

- DC Implementables
are special patterns of DC Standard Forms (due to A.P. Ravn).
- Within one pattern,
 - $\pi, \pi_1, \dots, \pi_n, n \geq 0$, denote **phases** of **the same** state variable X_i ,
 - φ denotes a state assertion not depending on X_i .
- θ denotes a **rigid** term.

- **Initialisation:**

$$[\] \vee [\pi] ; true$$

- **Sequencing:**

$$[\pi] \longrightarrow [\pi \vee \pi_1 \vee \dots \vee \pi_n]$$

- **Progress:**

$$[\pi] \xrightarrow{\theta} [\neg\pi]$$

- **Synchronisation:**

$$[\pi \wedge \varphi] \xrightarrow{\theta} [\neg\pi]$$

Recall: DC Implementables Cont'd

- **Bounded Stability:**

$$[\neg\pi] ; [\pi \wedge \varphi] \xrightarrow{\leq\theta} [\pi \vee \pi_1 \vee \dots \vee \pi_n]$$

- **Unbounded Stability:**

$$[\neg\pi] ; [\pi \wedge \varphi] \longrightarrow [\pi \vee \pi_1 \vee \dots \vee \pi_n]$$

- **Bounded initial stability:**

$$[\pi \wedge \varphi] \xrightarrow{\leq\theta} [\pi \vee \pi_1 \vee \dots \vee \pi_n]$$

- **Unbounded initial stability:**

$$[\pi \wedge \varphi] \longrightarrow [\pi \vee \pi_1 \vee \dots \vee \pi_n]$$

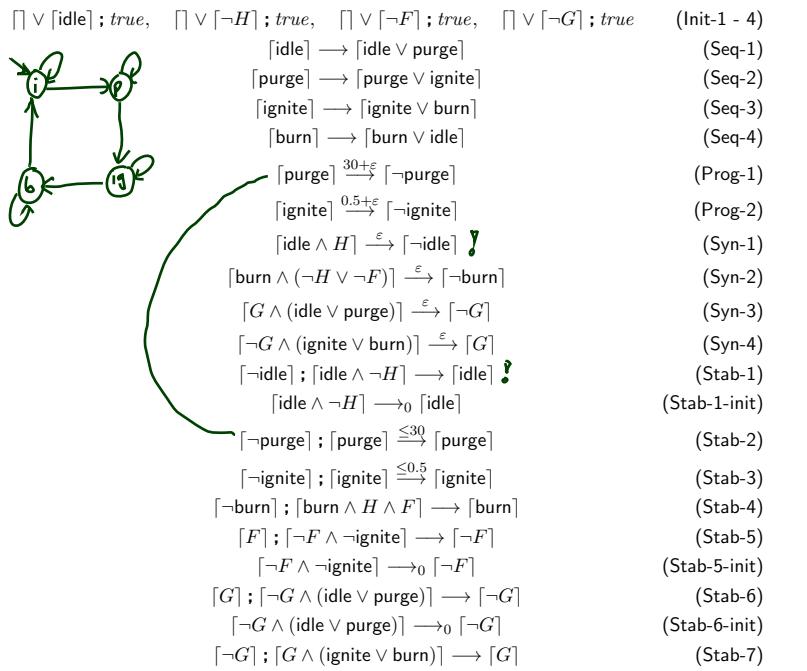
Recall: Control Automata

Model of Gas Burner controller as a system of four control automata:

- H : Boolean,
representing **heat request**, (input)
- F : Boolean,
representing **flame**, (input)
- C with $\mathcal{D}(C) = \{\text{idle}, \text{purge}, \text{ignite}, \text{burn}\}$,
representing the **controller**, (local)
- G : Boolean,
representing **gas valve**. (output)

Gas Burner Controller Specification

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Gas Burner Controller Correctness Proof

$$\text{GB-Ctrl} := \text{Init-1} \wedge \dots \wedge \text{Stab-7} \wedge \varepsilon > 0$$

Recall:

$$\text{Req} : \square(\ell \geq 60 \implies 20 \cdot \int L \leq \ell)$$

and (cf. [Olderog and Dierks, 2008])

$$\models \text{Req-1} \implies \text{Req}$$

for the **simplified**

$$\text{Req-1} := \square(\ell \leq 30 \implies \int L \leq 1).$$

$$\models \text{GB-Ctrl} \wedge A(\varepsilon) \implies \text{Req-1}.$$

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Here we show

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Lemma 3.15

$$\models \text{GB-Ctrl} \implies \square \left(\begin{array}{l} (\lceil \text{idle} \rceil \implies \int G \leq \varepsilon) \\ \wedge (\lceil \text{purge} \rceil \implies \int G \leq \varepsilon) \\ \wedge (\lceil \text{ignite} \rceil \implies \ell \leq 0.5 + \varepsilon) \\ \wedge (\lceil \text{burn} \rceil \implies \int \neg F \leq 2\varepsilon) \end{array} \right) (*)$$

Proof: Let \mathcal{I} be an interpretation, \mathcal{V} a valuation, and $[c, d]$ an interval with $\mathcal{I}, \mathcal{V}, [c, d] \models \text{GB-Ctrl}$. Let $[b, e] \subseteq [c, d]$.

ug. \square

- Case 1: $\mathcal{I}, \mathcal{V}, [b, e] \models \lceil \text{idle} \rceil$

$$\begin{aligned} & \lceil G \wedge (\text{idle} \vee \text{purge}) \rceil \xrightarrow{\varepsilon} \lceil \neg G \rceil && (\text{Syn-3}) \\ & \lceil G \rceil ; \lceil \neg G \wedge (\text{idle} \vee \text{purge}) \rceil \longrightarrow \lceil \neg G \rceil && (\text{Stab-6}) \\ & \text{conclude } \lceil \mathcal{I}, \mathcal{V}, [b, e] \models \square(\lceil G \rceil \implies \ell \leq \varepsilon) \wedge \neg \diamond(\lceil G \rceil ; \lceil \neg G \rceil ; \lceil G \rceil) \rceil \\ & \text{up again in idle phase} \end{aligned}$$

yes value doesn't open up again in idle phase

- Case 2: $\mathcal{I}, \mathcal{V}, [b, e] \models \lceil \text{purge} \rceil$ Analogously to case 1.

Lemma 3.15 Cont'd

$$\begin{array}{l} (\lceil \text{idle} \rceil \implies \int G \leq \varepsilon) \\ (\lceil \text{purge} \rceil \implies \int G \leq \varepsilon) \\ (\lceil \text{ignite} \rceil \implies \ell \leq 0.5 + \varepsilon) \\ (\lceil \text{burn} \rceil \implies \int \neg F \leq 2\varepsilon) \end{array}$$

- Case 3: $\mathcal{I}, \mathcal{V}, [b, e] \models \lceil \text{ignite} \rceil$

$$\begin{aligned} & \lceil \text{ignite} \rceil \xrightarrow{0.5+\varepsilon} \lceil \neg \text{ignite} \rceil && (\text{Prog-2}) \\ & \lceil \mathcal{I}, \mathcal{V}, [b, e] \models \ell \leq 0.5 + \varepsilon \rceil \end{aligned}$$

- Case 4: $\mathcal{I}, \mathcal{V}, [b, e] \models \lceil \text{burn} \rceil$

$$\begin{array}{l} \lceil \neg \text{ignite} \rceil \\ \lceil \neg \text{ignite} \rceil ; \lceil \neg \text{ignite} \rceil \\ \lceil \neg \text{ignite} \rceil ; \lceil \neg \text{ignite} \rceil ; \lceil \neg \text{ignite} \rceil \\ \lceil \neg \text{ignite} \rceil ; \lceil \neg \text{ignite} \rceil ; \lceil \neg \text{ignite} \rceil \end{array}$$

$$\begin{aligned} & \lceil \text{burn} \wedge (\neg H \vee \neg F) \rceil \xrightarrow{\varepsilon} \lceil \neg \text{burn} \rceil && (\text{Syn-2}) \\ & \lceil F \rceil ; \lceil \neg F \wedge \neg \text{ignite} \rceil \longrightarrow \lceil \neg F \rceil && (\text{Stab-5}) \end{aligned}$$

Lemma 3.16

$$\models \exists \varepsilon \bullet \text{GB-Ctrl} \implies \underbrace{\square(\ell \leq 30 \implies \int L \leq 1)}_{\text{Req-1}}$$

Proof Sketch

Choose $\mathcal{I}, \mathcal{V}, [b, e]$ s.t. $\mathcal{I}, \mathcal{V}, [b, e] \models \text{GB-Ctrl} \wedge \ell \leq 30$.

Distinguish 5 cases:

$$\begin{aligned} \mathcal{I}, \mathcal{V}, [b, e] &\models \Gamma ? & (0) \\ \vee (\Gamma_{\text{idle}}; \text{true} \wedge \ell \leq 30) && (1) \\ \vee (\Gamma_{\text{purge}}; \text{true} \wedge \ell \leq 30) && (2) \\ \vee (\Gamma_{\text{ignite}}; \text{true} \wedge \ell \leq 30) && (3) \\ \vee (\Gamma_{\text{burn}}; \text{true} \wedge \ell \leq 30) && (4) \end{aligned}$$

Lemma 3.16 Cont'd

- Case 0: $\mathcal{I}, \mathcal{V}, [b, e] \models \top \checkmark$
- Case 1: $\mathcal{I}, \mathcal{V}, [b, e] \models [\text{idle}] ; \text{true} \wedge \ell \leq 30$

$$[\text{idle}] \longrightarrow [\text{idle} \vee \text{purge}] \quad (\text{Seq-1})$$

$$[\neg \text{purge}] ; [\text{purge}] \xrightarrow{\leq 30} [\text{purge}] \quad (\text{Stab-2})$$

$$\begin{aligned} &\hookrightarrow \mathcal{I}, \mathcal{V}, [b, e] \models [\text{idle}] \vee [\text{idle}] ; [\text{purge}] \\ 3.15 \quad &\hookrightarrow \mathcal{I}, \mathcal{V}, [b, e] \models \int L \leq \varepsilon \vee \int L \leq \varepsilon ; \int L \leq \varepsilon \\ &\hookrightarrow \mathcal{I}, \mathcal{V}, [b, e] \models \int L \leq 2\varepsilon \end{aligned}$$

Thus $\boxed{\varepsilon \leq 0.5}$ is sufficient for Req-1 in this case.

Lemma 3.16 Cont'd

- Case 2: $\mathcal{I}, \mathcal{V}, [b, e] \models [\text{burn}] ; \text{true} \wedge \ell \leq 30$

$$\begin{aligned}
 & [\text{burn}] \longrightarrow [\text{burn} \vee \text{idle}] \quad (\text{Seq-4}) \\
 \xrightarrow{\quad} & \mathcal{I}, \mathcal{V}, [b, e] \models (\Gamma_{\text{burn}}, \Gamma_{\text{idle}}; \underbrace{\text{true}}_{(1)}, \ell \leq 30) \\
 3.15, (1) \xrightarrow{\quad} & \mathcal{I}, \mathcal{V}, [b, e] \models (\text{JL} \leq 2\varepsilon \vee \text{JL} \leq 2\varepsilon; \text{JL} \leq 2\varepsilon), \ell \leq 30 \\
 \hookrightarrow & \mathcal{I}, \mathcal{V}, [b, e] \models \text{JL} \leq 4\varepsilon \\
 \text{Thus } & \boxed{\varepsilon \leq 0.25} \text{ sufficient for Reg-7 in this case.}
 \end{aligned}$$

Lemma 3.16 Cont'd

- Case 3: $\mathcal{I}, \mathcal{V}, [b, e] \models [\text{ignite}] ; \text{true} \wedge \ell \leq 30$

$$\begin{aligned}
 & [\text{ignite}] \longrightarrow [\text{ignite} \vee \text{burn}] \quad (\text{Seq-3}) \\
 \xrightarrow{\quad} & \mathcal{I}, \mathcal{V}, [b, e] \models (\Gamma_{\text{ignite}}, \Gamma_{\text{burn}}; \underbrace{\text{true}}_{(2)}, \ell \leq 30) \\
 3.15, (2) \xrightarrow{\quad} & \mathcal{I}, \mathcal{V}, [b, e] \models (\text{JL} \leq 0.5 + \varepsilon \vee \text{JL} \leq 0.5 + \varepsilon; \text{JL} \leq 4\varepsilon), \ell \leq 30 \\
 \hookrightarrow & \mathcal{I}, \mathcal{V}, [b, e] \models \text{JL} \leq 0.5 + 5\varepsilon \\
 \text{So } & \boxed{\varepsilon \leq 0.1} \text{ sufficient in this case.}
 \end{aligned}$$

Lemma 3.16 Cont'd

- Case 4: $\mathcal{I}, \mathcal{V}, [b, e] \models [\text{purge}] ; \text{true} \wedge \ell \leq 30$

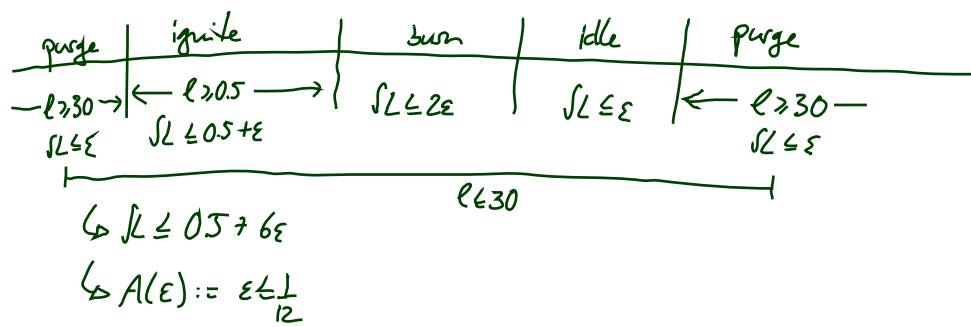
$$\begin{array}{c} [\text{purge}] \longrightarrow [\text{purge} \vee \text{ignite}] \\ \xrightarrow[3) \quad \text{Seq-2}]{3.15} \mathcal{I}, \mathcal{V}, [b, e] \models \ell \leq 0.5 + 6\varepsilon \end{array}$$

Thus $\boxed{\varepsilon \leq \frac{1}{12}}$ is sufficient for Req-7 in this case.

Correctness Result

Theorem 3.17.

$$\models (\text{GB-Ctrl} \wedge \varepsilon \leq \frac{1}{12}) \implies \text{Req}$$



Discussion

- We used only

'Seq-1', 'Seq-2', 'Seq-3', 'Seq-4',
'Prog-2', 'Syn-2', 'Syn-3',
'Stab-2', 'Stab-5', 'Stab-6'.

What about

$$\text{Prog-1} = [\text{purge}] \xrightarrow{30+\varepsilon} [\neg\text{purge}]$$

for instance?

*Naja, there is the requirement (not voted down)
that the system does something finally,
e.g. get the heating going on request.*

RDC in Discrete Time Cont'd

Restricted DC (RDC)

$$F ::= [P] \mid \neg F_1 \mid F_1 \vee F_2 \mid F_1 ; F_2$$

where P is a state assertion, but with **boolean** observables **only**.

Note:

- No global variables, thus don't need \mathcal{V} .
- *chop is there*
 - no \int , no ℓ (in general)
 - no predicates, no function symbols (in general)
 - $\diamond F \dots ?$
 - $[? \dots ?]$

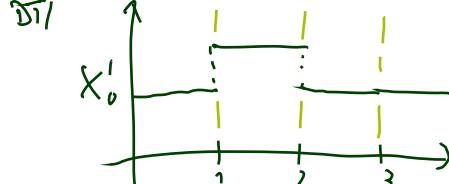
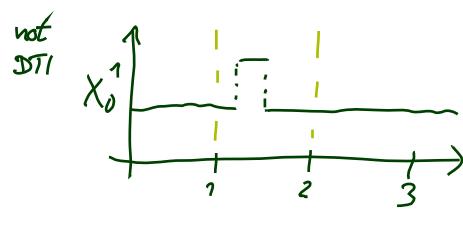
Discrete Time Interpretations

- An interpretation \mathcal{I} is called **discrete time interpretation** if and only if, for each state variable X ,

$$X_{\mathcal{I}} : \text{Time} \rightarrow \mathcal{D}(X)$$

with

- $\text{Time} = \mathbb{R}_0^+$,
- all discontinuities are in \mathbb{N}_0 .



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Discrete Time Interpretations

- An interpretation \mathcal{I} is called **discrete time interpretation** if and only if, for each state variable X ,

• We say $\mathcal{I}, [b, e] \models F$

$$X_{\mathcal{I}} : \text{Time} \rightarrow \mathcal{D}(X)$$

if
 $\int_b^e P_{\mathcal{I}}(t) dt = (e-b)$
 $\wedge (e-b) > 0$

with

- Time = \mathbb{R}_0^+ ,
- all discontinuities are in \mathbb{N}_0 .

- An interval $[b, e] \subset \text{Intv}$ is called **discrete** if and only if $b, e \in \mathbb{N}_0$.

- We say (for a discrete time interpretation \mathcal{I} and a discrete interval $[b, e]$)

$$\mathcal{I}, [b, e] \models F_1 ; F_2$$

if and only if there exists $m \in [b, e] \cap \mathbb{N}_0$ such that

$$\mathcal{I}, [b, m] \models F_1 \quad \text{and} \quad \mathcal{I}, [m, e] \models F_2$$

Differences between Continuous and Discrete Time

- Let P be a state assertion.

	Continuous Time	Discrete Time
$\models^? ([P]; [P]) \implies [P]$	✓ ✓	✓ ✓
$\models^? [P] \implies ([P]; [P])$	✓ ✓	✗ ✗

only chop-point candidates
are $m=1$ and $m=2$
but then

$$m-b=0 \text{ or } e-m=0$$

- In particular: $\ell = 1 : \iff ([1] \wedge \neg([1]; [1]))$ (in discrete time).

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Expressiveness of RDC

- $\ell = 1 \iff [1] \wedge \neg([1]; [1])$
 - $\ell = 0 \iff \neg[1]$
 - $true \iff \ell=0 \vee \neg(\ell=0)$
 - $\int P = 0 \iff [\neg P] \vee \ell=0$
 - $\int P = 1 \iff (\int P = 0) \wedge (\neg P \wedge \ell=1) \wedge (\int P = 0)$
 - $\int P = k+1 \iff (\int P = k) \wedge (\int P = 1)$
 - $\int P \geq k \iff (\int P = k) \wedge true$
 - $\int P > k \iff \int P \geq k+1$
 - $\int P \leq k \iff \neg(\int P > k)$
 - $\int P < k \iff \int P \leq k-1$
- so still $\Diamond F = true; F; true$
in RDC
- where $k \in \mathbb{N}^+$

Decidability of Satisfiability/Realisability from 0

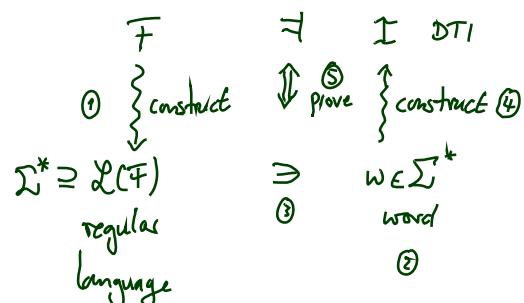
Theorem 3.6.

The satisfiability problem for RDC with discrete time is decidable.

Theorem 3.9.

The realisability problem for RDC with discrete time is decidable.

RDC formula F .



- $\mathcal{L}(F) = \emptyset \Rightarrow F \text{ not SAT}$
- $\mathcal{L}(F) = \emptyset$ is decidable

References

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- [Chaochen and Hansen, 2004] Chaochen, Z. and Hansen, M. R. (2004).
Duration Calculus: A Formal Approach to Real-Time Systems. Monographs in Theoretical Computer Science. Springer-Verlag. An EATCS Series.
- [Olderog and Dierks, 2008] Olderog, E.-R. and Dierks, H. (2008). *Real-Time Systems - Formal Specification and Automatic Verification*. Cambridge University Press.