## Tutorial for Cyber-Physical Systems - Discrete Models Exercise Sheet 10

This is a bonus sheet to recap some of the important concepts introduced earlier in the lecture. If you have some time during or after the break, you can use this sheet to practice - and to catch up with the points if needed.

## Exercise 1*: LT Properties

The goal of this task is to learn to identify the different types of LT properties.
Consider the following LT properties with $A P=\{a, b\}$.
$\left(P_{1}\right)$ Always (at any point of time) $a$ or $b$ holds.
$\left(P_{2}\right)$ Either $a$ holds exactly once, or $b$ never holds.
$\left(P_{3}\right)$ If $a$ holds, then $b$ will never hold in the next step.
$\left(P_{4}\right)$ Every time $a$ holds there will be eventually a point of time where $b$ holds.
$\left(P_{5}\right)$ The atomic propositions $a$ and $b$ never hold at the same time.
$\left(P_{6}\right)$ If $a$ holds infinitely often, then $b$ holds infinitely often.
$\left(P_{7}\right)$ There are only finitely many points of time where $a$ holds.
$\left(P_{8}\right)$ True
For each property $P_{i}$ complete the following tasks:
(a) Formalize $P_{i}$ using set notation.
(b) Determine if $P_{i}$ is an invariant. In that case provide the invariant condition.
(c) Determine if $P_{i}$ is a safety property. Explain why or why not.
(d) Determine if $P_{i}$ is a liveness property. Explain why or why not.

Consider the following locking protocol. The initial value of the variable x is 0 .


Note: There is a difference between $\mathrm{x}:=1$ and $\mathrm{x}==1$. The edge labeled with $\mathrm{x}:=1$ can always be taken (as there is no guard) and it modifies the value of $x$. On the other hand, the edge with $\mathrm{x}==1$ can only be taken when x has the value 1 , and it does not modify the value of $x$.
(a) Draw the program graph $P_{1} \| \mid P_{2}$, i.e. the program graph for the interleaving of $P_{1}$ and $P_{2}$.
(b) Draw the reachable part of the transition system $\mathcal{T}_{P_{1} \| P_{2}}$ for the interleaving of the programs. Use the atomic propositions $\left\{\right.$ crit $_{1}$, crit $\left._{2}\right\}$ that are satisfied, whenever process 1 respectively process 2 are in their critical section.
(c) Does the protocol satisfy the mutual exclusion property? Explain your answer in sufficient detail.
(d) Is this a reasonable protocol for parallel programs? Explain your answer in sufficient detail.

## Exercise 3*: Mutual Exclusion without Request

6 Bonus Points
The goal of this exercise is to help you understand in detail the SOS-rules for parallel compositions.
The transition systems below describe a mutual-exclusion protocol with an arbiter. In contrast to the system discussed in the lecture, we omit the request action.

$T S_{1}$


Arbiter

$T S_{2}$
（a）Draw the transition system for the pure interleaving $T S_{1} \|| | S_{2}$ ．There must be no synchronization between the two transition systems．
For every transition in the interleaving，justify why it must exist using one of the two SOS－rules for pure interleaving．

Example：The interleaving must contain the transition 〈idle，idle〉 $\xrightarrow{\text { enter }}\langle$ crit，idle〉 due to the SOS－rule

$$
\frac{\text { idle } \xrightarrow{\text { enter }} 1 \text { crit }}{\langle\text { idle, idle }\rangle \xrightarrow{\text { enter }}\langle\text { crit, idle }\rangle}
$$

where $\rightarrow_{1}$ is the transition relation for $T S_{1}$ ．This is an instance of the first of the two SOS－rules，

$$
\frac{s_{1} \xrightarrow[\rightarrow]{\alpha} s_{1}^{\prime}}{\left\langle s_{1}, s_{2}\right\rangle \xrightarrow{\alpha}\left\langle s_{1}^{\prime}, s_{2}\right\rangle}
$$

where we set $s_{1}=$ idle，$\alpha=$ enter，$s_{1}^{\prime}=$ crit and $s_{2}=$ idle．
（b）Draw the transition system for the parallel composition $\left(T S_{1} \| \mid T S_{2}\right) \|$ Arbiter of the transition system from（a）with the arbiter．The transition systems must synchronize（＂handshake＂）on the actions \｛enter，exit\}.
For every transition in the composition，justify why it must exist using one of the three SOS－rules for the synchronization operator．

## Exercise 4＊：Hardware Circuit

4 Bonus Points
Consider the following sequential hardware circuit．


Provide the labeled transition system of this hardware circuit（i．e．，states are labeled by sets of atomic propositions，transitions are not labeled）．The states are the evaluations of the input $x$ and the register $r$ ．The transitions represent the stepwise behavior of the circuit．The values of the input $x$ change nondeterministically．The atomic propositions $\{X, Y, R\}$ stand for $x=1, y=1$ and $r=1$ ，respectively．Initially the register $r$ has the value 0 （false）．

For your reference：$D=$ AND gate，$D=$ OR gate，$D^{\circ}=$ NOT gate

